

JK LAKSHMIPAT UNIVERSITY

DIGITAL CIRCUIT AND SYSTEMS  
(EE1120)

Activity 13

Design D Flip Flop using VHDL language.

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# AIM: Design and Simulation of D Flip Flop using data flow modelling in VHDL language using Xilinx ISE software.

SOFTWARE REQUIRED: Xilinx ISE tool in your device.

THEORY: A D flip-flop is a type of sequential logic circuit that stores a single bit of data. It has two stable states (0 or 1) and is capable of toggling between these states based on certain input conditions. The fundamental operation of a D flip-flop involves the following key components:

* Data Input (D): The D input is the primary input of the flip-flop. It determines the state (0 or 1) that the flip-flop will store. When the D input is high (logic 1), the flip-flop will store a 1, and when the D input is low (logic 0), the flip-flop will store a 0.
* Clock Input (CLK): The clock input controls the timing of when the flip-flop samples the D input. The flip-flop will only update its stored state when the clock input transitions from one state to another (e.g., from low to high or from high to low).
* Output (Q): The Q output represents the current state of the flip-flop. It reflects the value stored by the flip-flop based on the last clock transition.
* Inverted Output (/Q): The inverted output (/Q) is the complement of the Q output. When Q is high, /Q is low, and vice versa.

The operation of a D flip-flop can be summarized as follows:

* When the clock input transitions (e.g., from low to high), the flip-flop samples the value of the D input.
* If the D input is high, the flip-flop sets its output Q to high.
* If the D input is low, the flip-flop sets its output Q to low.
* The output Q remains unchanged until the next clock transition occurs, at which point it will reflect the sampled value of the D input again.

D flip-flops are commonly used in digital circuits for various purposes such as data storage, synchronization, and control. They are building blocks for more complex sequential logic circuits, including counters, shift registers, and state machines.

There are different variations of D flip-flops, including positive-edge-triggered and negative-edge-triggered types, which determine whether the flip-flop samples the D input on the rising edge or falling edge of the clock signal, respectively. Additionally, synchronous and asynchronous types of D flip-flops exist, each with different timing requirements and behaviors.

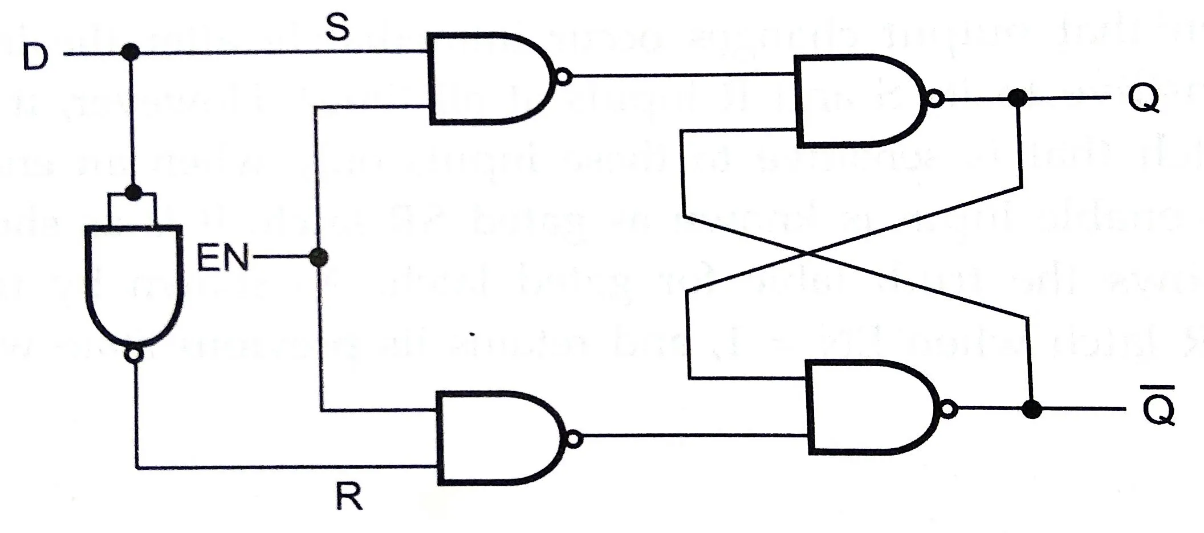


Figure 1

OBSERVATION: The observed outputs of D Flip Flops are as follows:

USING DATAFLOW:

VHDL Code: RTL Diagram:

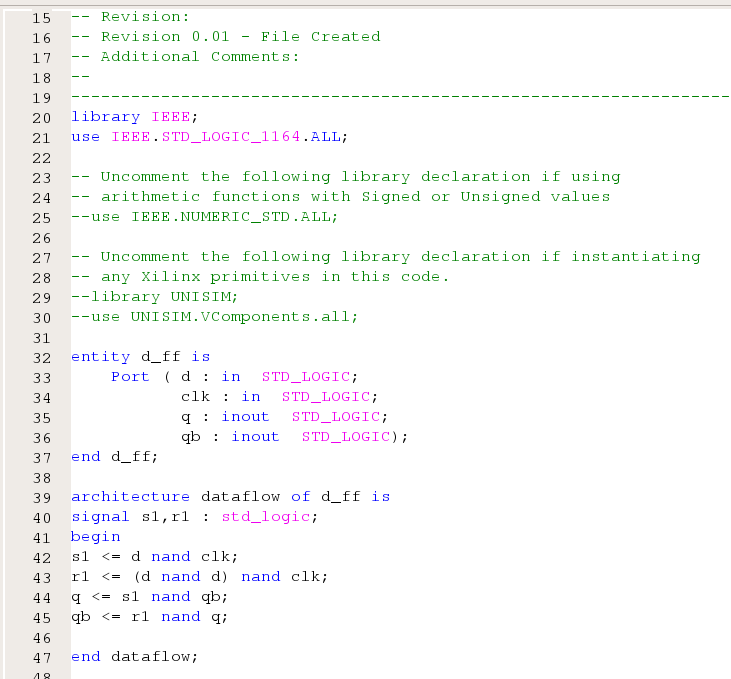
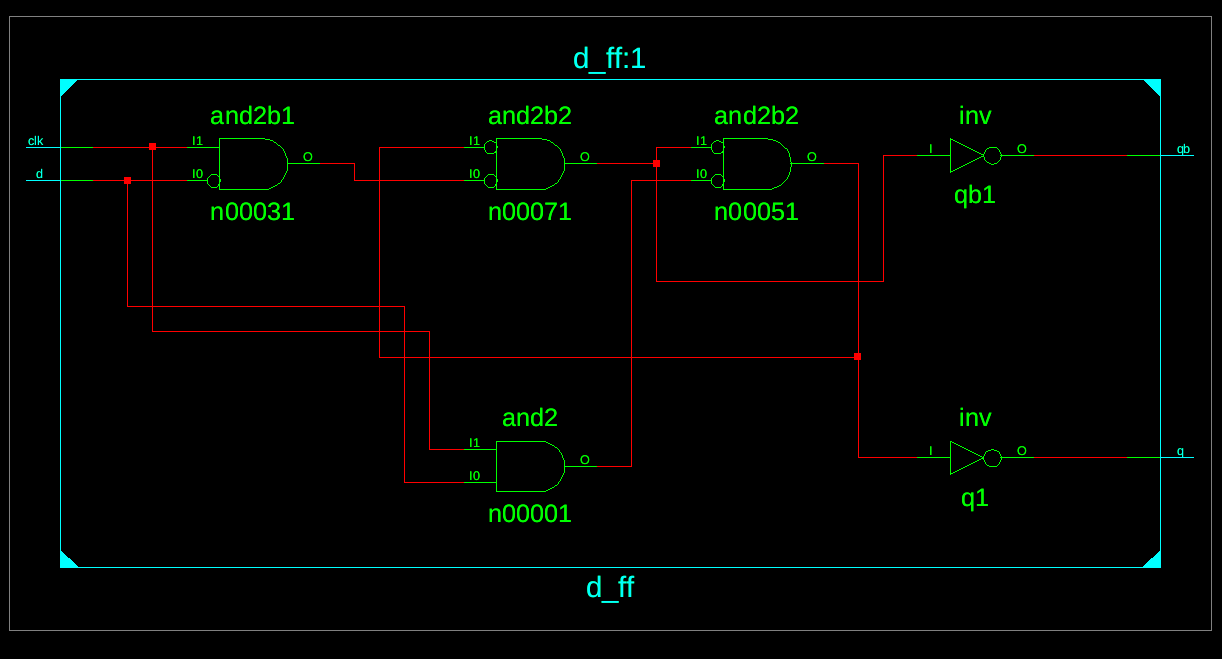
 

Figure 2 Figure 3

Test Bench Code:

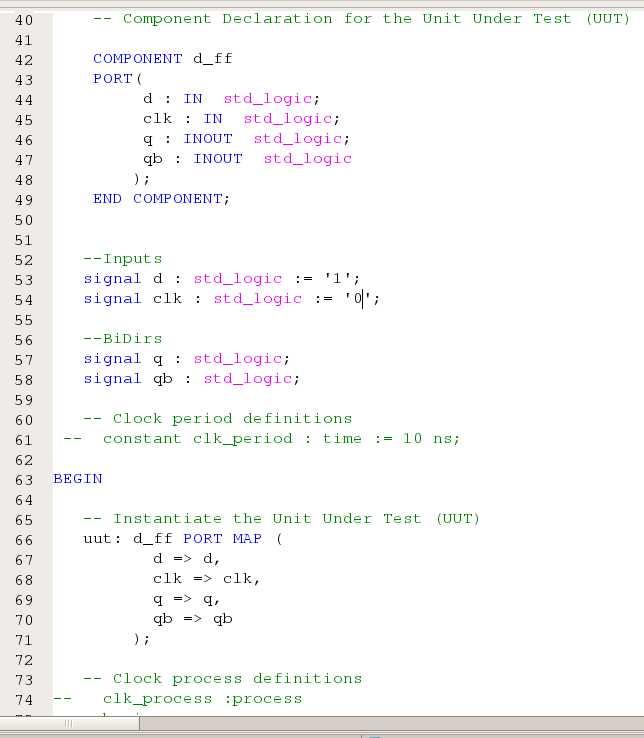


Figure 4

Waveform:

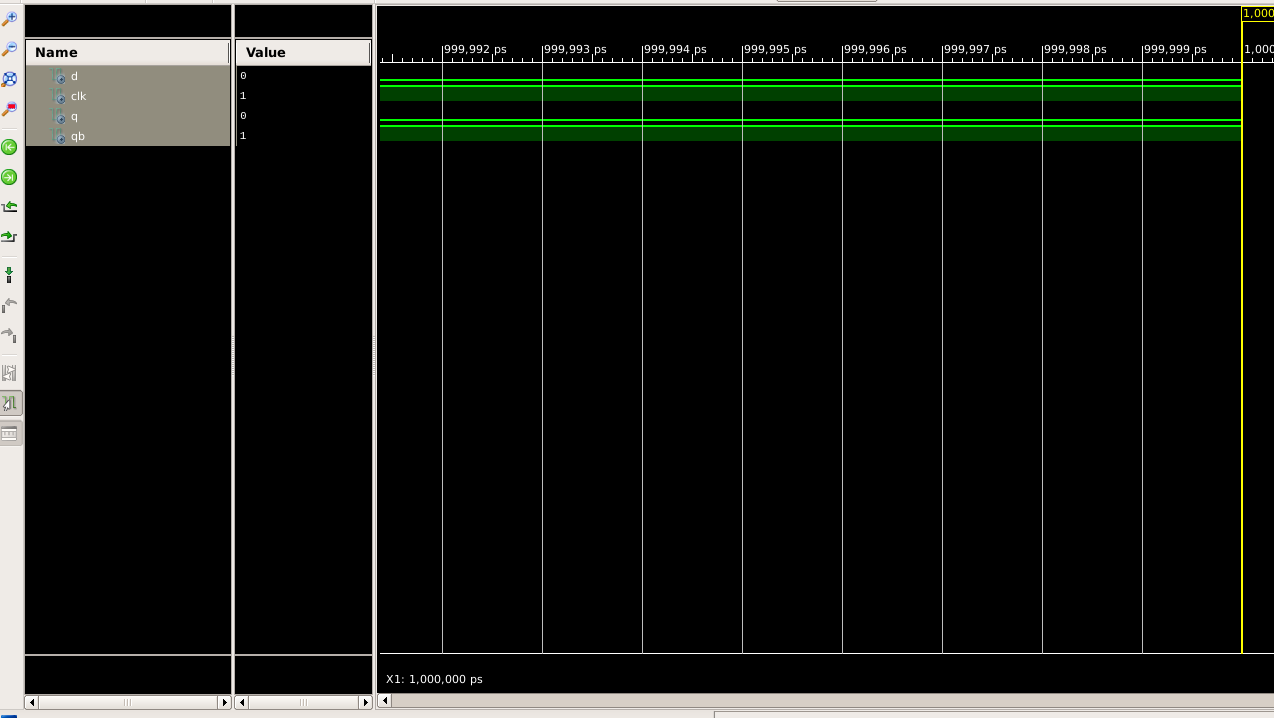


Figure 5

Here the yellow line in figure 5 represents the input (d and clock = 0 and 1 ) and therefore the output (q and q (bar) ) will be represented as the output which in this case is 0 and 1. The truth table ford flip flop until our clock’s input is 0 can be concluded by this observation.

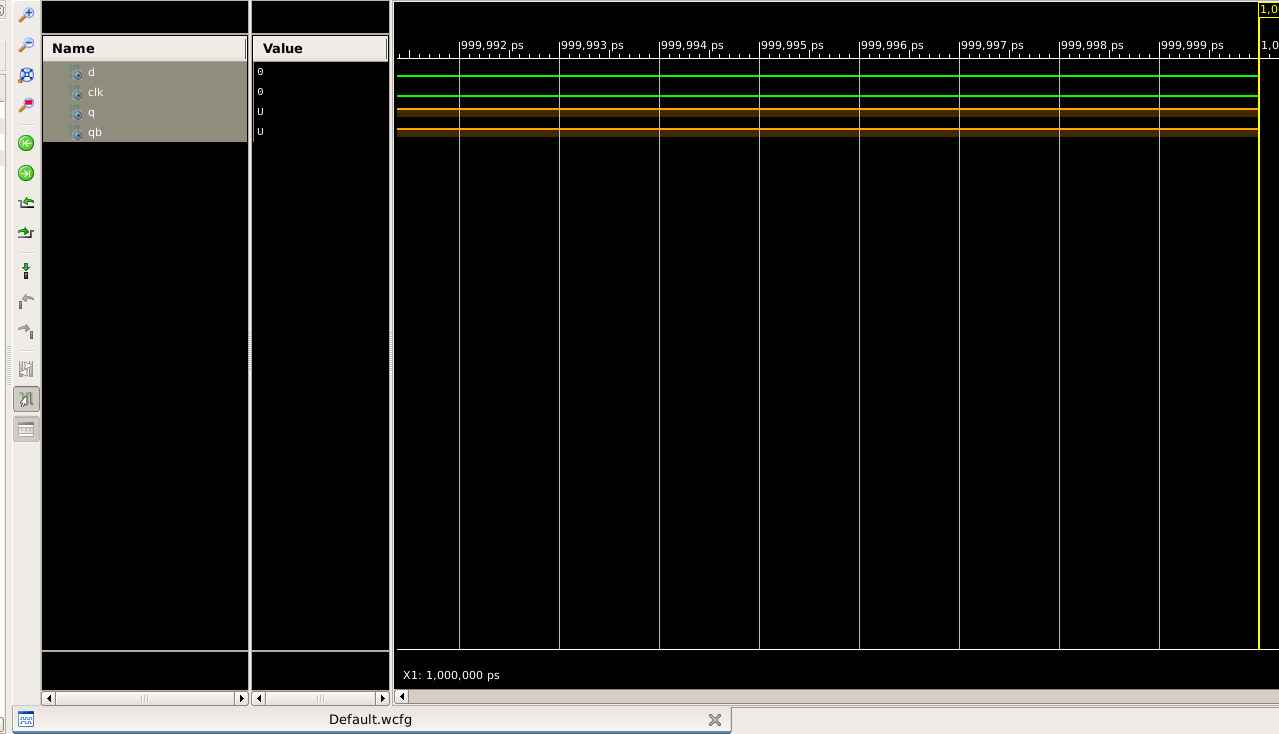


Figure 6

Here the orange line in figure 6 represents the input of clock is 0 and therefore the output will be the previous state. Hence, the truth table of D Flip Flop is as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| D | Clock | Q(n+1) | Compliment of Q(n+1) |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |
| x | 0 | Qn | (Qn) bar |
| x | 0 | Qn | (Qn) bar |

Table 1

Further we can also make the characteristic table and through that table we can easily conclude the characteristic equation :

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| D | Qn | Clock | Q(n+1) | Compliment of Q(n+1) |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |

Table 2

The characteristic equation that can be drawn as :

Q(n+1) = D

After forming Excitation table, the same equation can also be drawn.

# RESULT: We have concluded the truth table, characteristic table, characteristic equation, and excitation table of d flip flop using VHDL language in Xilinx ISE Tool.

APPLICATION IN DAILY LIFE:

* **Memory Devices:** D flip-flops are essential components of memory devices like RAM (Random Access Memory) and registers. RAM in computers stores data temporarily while the system is running. Registers are used for storing data temporarily within the CPU during processing. So, every time you use a computer or any digital device that requires memory, you're indirectly utilizing D flip-flops.
* **Communication Systems**: In communication systems such as wireless networks, D flip-flops are used in various components like modems and routers. These components utilize flip-flops in data synchronization, timing recovery, and other functionalities critical for reliable data transmission.
* **Control Systems:** D flip-flops are used in control systems for sequential logic and state memory. They play a role in maintaining the state of the system, ensuring proper sequencing of events, and implementing control algorithms.
* **Digital Clocks and Timers:** D flip-flops are utilized in digital clocks and timers to store and manipulate time data. They help in counting seconds, minutes, and hours accurately, ensuring precise timekeeping in various devices ranging from simple alarm clocks to sophisticated industrial control systems.